ABSTRACT OF THE DISCLOSURE

A processor (e.g., a co-processor) comprising a decoder adapted to decode instructions from a first instruction set in a first mode and a second instruction set in a second mode. A pre-decoder coupled to the decoder, and operates in parallel with the decoder, determines the mode of operation for the decode logic for subsequent instructions. In particular, the decode logic operating in a current mode concurrently with the pre-decoder detecting a predetermined prefix, which indicates a subsequent instruction is a system command. Upon detecting this predetermined prefix, the decoder decodes the system command accordingly.